

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Michael I. Catherwood

Serial No.: 09/870,711

Filing Date: June 1, 2001

Group Art Unit: 3124

Examiner: David H. Malzahn

Title: **MAXIMALLY NEGATIVE SIGNED  
FRACTIONAL NUMBER MULTIPLICATION**



MAIL STOP - RCE  
Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

I hereby certify that this Information Disclosure Statement is being deposited with the United States Postal Service as Express Mail **EV351286597US** addressed to: Mail Stop RCE, Commissioner of Patents, Alexandria, VA 22313-1450, on March 23, 2005.

  
Adesewa Faleti

Dear Sir:

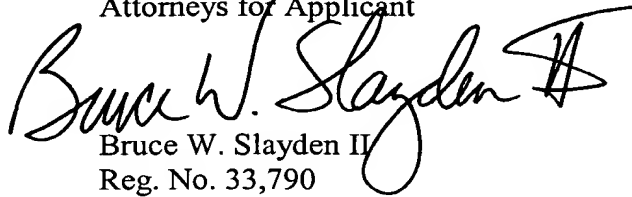
**INFORMATION DISCLOSURE STATEMENT**

Applicant respectfully requests, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the references listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. Copies of the references are enclosed for the Examiner's convenience. Furthermore, pursuant to 37 C.F.R. §§1.97 (g) and (h), no representation is made that these references are material to the patentability of the present application.

Applicant believes no fees are due at this time, however, the Commissioner is hereby authorized to charge any fees required to Deposit Account No. 50-2148 of Baker Botts L.L.P.

Respectfully submitted,

BAKER BOTTS L.L.P.  
Attorneys for Applicant

  
Bruce W. Slayden II  
Reg. No. 33,790

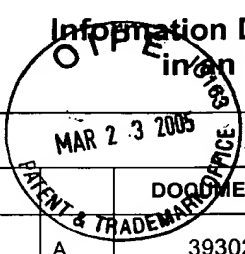
Date: March 23, 2005

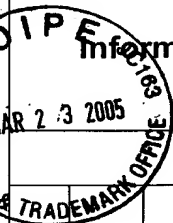
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PTO-1449		Application No. <b>09/870,711</b>		Applicant(s) <b>Catherwood</b>			
<b>Information Disclosure Citation in an Application</b> 		Docket Number <b>068354.1446</b>		Group Art Unit <b>2124</b>	Filing Date <b>June 1, 2001</b>		
		<b>U.S. PATENT DOCUMENTS</b>					
	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
A.	3930253	12/30/75	Maida	340	347	1/24/74	
B.	4408274	10/4/83	Wheatley et al.	364	200	9/29/80	
C.	4709324	11/24/87	Kloker	364	200	11/27/85	
D.	4945507	7/31/90	Ishida et al.	708	530	6/12/89	
E.	5386563	1/31/95	Thomas, deceased	395	650	10/13/92	
F.	5450027	9/12/95	Gabara	326	98	4/8/94	
G.	5561384	10/1/96	Reents et al.	327	108	11/8/95	
H.	5623646	4/22/97	Clarke	395	560	9/12/95	
I.	5701493	12/23/97	Jaggar	395	734	8/3/95	
J.	5974549	10/26/99	Golan	713	200	3/27/97	
K.	6055619	4/25/00	North et al.	713	36	2/7/97	
L.	6282637	8/28/01	Chan et al.	712	223	12/2/98	
M.	6694398	2/17/04	Zhao et al.	710	260	4/30/01	
N.	6728856	4/27/04	Grosbach et al.	711	202	6/1/01	
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
O.	01037124 A	2/1989	JP (w/abstract)	H03M	001/82		X
P.	0 554 917 A2	8/11/93	EP	G06F	9/26	X	
Q.	96/11443	4/18/96	WO	G06F	15/78	X	
R.	0 855 643 A1	07/29/98	EP	G06F	9/30	X	
S.	0 992 888	12/04/00	EP	G06F	9/32	X	
NON-PATENT DOCUMENTS - DOCUMENT (Including Author, Title, Source, and Pertinent Pages)							
T.	Moon B I et al.: "A 32-bit RISC Microprocessor with DSP Functionality: Rapid Prototyping" IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Institute of Electronics Information and Comm. Eng. Tokyo, JP, vol. E84-A no. 5, pages 1339-1347, XP001060025 ISSN: 0916-8508						May 2001
U.	Turley J: "Balancing Conflicting Requirements When Mixing RISC, DSPs" Computer Design, Pennwell Publ. Littleton, Massachusetts, IS, vol. 37, no. 10, pages 46, 48, 50-53, XP000860706 ISSN:0010-4566						October 1998
V.	Levy M: "Microprocessor and DSP Technologies Unite for Embedded Applications" EDN Electrical Design News, Cahners Publishing Co., Newtown Massachusetts, US, no. Europe, pages 73-74, 76, 78-80, XP000779113 ISSN: 0012-7515						2 March 1998
EXAMINER				DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.							

PTO-1449		Application No. 09/870,711		Applicant(s) Catherwood			
 <b>Information Disclosure Citation in an Application</b>		Docket Number 068354.1446		Group Art Unit 2124	Filing Date June 1, 2001		
<b>U.S. PATENT DOCUMENTS</b>							
	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
A.							
B.							
C.							
D.							
E.							
F.							
G.							
<b>FOREIGN PATENT DOCUMENTS</b>							
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO	
H.	0 992 889	12/14/00	EP	G06F	9/32	X	
I.							
J.							
<b>NON-PATENT DOCUMENTS - DOCUMENT (Including Author, Title, Source, and Pertinent Pages)</b>							
K.	Intel, Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, , Pages 3-1, 3-2, 3-15, 14-1 to 14-30, 18-7, and 25-289 to 25-292					1995	
L.	Intel, Embedded Intel486 Processor Family Developer's Manual, pgs. 2-2, 3-17, 3-37, 4-5, 4-6, 10-1 to 10-12, 12-1 to 12-10					10/1997	
M.	Moore, M "Z80 Family Interrupt Structure". Barleywood (online), retrieved from the internet <URL: <a href="http://www.gaby.de/z80/1653.htm">http://www.gaby.de/z80/1653.htm</a> >					1997	
N.	PCT Search Report based on PCT/US02/16706, 6 pages					Mailed 9/27/02	
O.	PCT Search Report based on PCT/US02/16705, 7 pages					Mailed 9/9/02	
P.	PCT Search Report based on PCT/US02/16921, 4 pages					Mailed 10/18/02	
Q.	SPARC, International, Inc., "The SPARC Architecture Manual", Version 8, pp 1-303					1992	
R.	Weaver, et al., SPARC International, Inc. "The SPARC Arcitecture Manual", Version 9, pp. xiv, 137, 146-147, 200-204, 221-222, 234-236, 299					1994-2000	
S.	Free On-Line Dictionary of Computing (FOLDOC). <a href="http://wombat.doc.ic.ac.uk/foldoc/">http://wombat.doc.ic.ac.uk/foldoc/</a> Search term: program counter, 1 page					1995	
EXAMINER				DATE CONSIDERED			
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